REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1, 2, 4-8, 10-20, and 22-28 are currently pending, with Claims 11-20 being withdrawn as directed to non-elected inventions. Claims 1 and 2 have been amended; Claim 21 has been canceled; and Claims 22-28 have been added by the present amendment. The changes to the claims are supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, Claim 21 was rejected under 35 U.S.C. § 112, second paragraph; Claims 1, 2, 7, 8, and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 3,866,029 to Chevalier et al. (hereinafter "the '029 patent"); Claims 4-6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the '029 patent in view of U.S. Patent No. 5,222,142 to Kent (hereinafter "the '142 patent"); and Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the '029 patent.

Applicants respectfully submit that the rejections of Claim 21 under 35 U.S.C. § 112 and 35 U.S.C. § 102 are rendered moot by the present cancellation of Claim 21.

Amended Claim 1 is directed to a random number generator, comprising: (1) a counter circuit configured to be supplied with a clock signal and a random signal, and to provide a count value of the clock signal with respect to a transition of the random signal; and (2) a first latch circuit configured to latch the count value with respect to the transition of the random signal, and to output a first random number signal. Further, Claim 1 has been amended to clarify that the counter circuit is a one-bit counter, the count value of which alternates between a high level and a low level every one count, the counter circuit having a

clock enable input to which the random number signal is supplied. The changes to Claim 1 are supported by the originally filed specification and do not add new matter.[1]

The '029 patent is directed to a random number generator for generating a sequence of binary random numbers whose expected value is controlled by an input digital number. As shown in the only figure in the '029 patent, the '029 patent discloses a binary counter 20, a latch 21, and a random bits generator 11. In particular, the '029 patent discloses that the binary counter 20 has four inputs: a clear input 14, a count input 16, a clock input, and an enable input 17. Further, as shown in the figure, the '029 patent discloses that the output 12 of the random bits generator 11 is input to the clear input of the binary counter, while the count input of the binary counter receives the inversion of the random signal 12, via the inverter 22.

In particular, the '029 patent discloses a four-bit counter 20 that requires a counter clear signal for operation. When the signal given to the enabling input 17 from the NB_i signal 13 is one and the signal given to the clear input 14 is one, the output C_i will be reset to zero. On the other hand, if the signal given to the count input 16 is one, the C_i output 25 will be reset to a clock pulse number that is fed to the clock input of the binary counter 20 from the clock. In other words, the binary counter 20 counts the clock pulse number when the RB_i output 12 is in the zero state. Thus, if the binary counter is not reset by the counter clear signal, the range of errors will be up to 16 bits. Further, Applicants note that in binary counter 20 disclosed by the '029 patent, misalignment of the input timing may occur such that the state of the clear and count inputs is either 00 or 11. Thus, if another clock signal is fed to the binary counter 20 when the binary counter 20 is in one of these states, the binary counter 20 cannot override the counter value even if a new random signal is fed to the binary

[1] See, e.g., Figure 1 and the discussion related thereto in the specification.

counter. Thus, the binary counter can't produce the appropriate random number. Applicants note that this misalignment is caused by having two inputs to the binary counter.

However, Applicants respectfully submit that the '029 patent fails to disclose a counter circuit that is a one-bit counter, the count value of which alternates between a high level and a low value every one count, as recited in Claim 1.

Further, Applicants respectfully submit that the '029 patent fails to disclose a counter circuit having a clock enable input to which the random signal is supplied, as required by amended Claim 1. As discussed above, the '029 patent discloses a random signal input to the clear input of the binary counter, while the enable input is fed by the NB_i signal 13. The NB_i signal 13 indicates if the bit RB_i is independent of the previous bit RB_{i-1}.

For the reasons stated above, Applicants respectfully submit that the rejection of Claim 1 (and all similar rejected dependent claims) is rendered moot by the present amendment to Claim 1.

Regarding the rejection of dependent Claims 4-6 under 35 U.S.C. § 103(a), Applicants respectfully submit that the '142 patent fails to remedy the deficiencies of the '029 patent, as discussed above. In particular, Applicants respectfully submit that the '142 patent fails to disclose the counter circuit recited in amended Claim 1. Accordingly, Applicants respectfully submit that the rejection of dependent Claims 4-6 is rendered moot by the present amendment to Claim 1.

Applicants respectfully submit that the rejection of Claim 10 under 35 U.S.C. § 103(a) is rendered moot by the present amendment to Claim 1.

The present amendment also sets forth new Claims 22-28 for examination on the merits. New independent Claim 22 is directed to a random number generator, comprising: (1) a counter circuit configured to be supplied with a clock signal and a random signal, and to provide a counter value of the clock signal with respect to a transition of the random signal;

(2) a first latch circuit configured to latch the count value with respect to the transition of the random signal, and to output a first random number signal; and (3) a source for the random signal adapted to produce said random signal having a characteristic in which power spectrum intensity decreases with increasing frequency. Further, Claim 22 clarifies that the source comprises an oscillation circuit using a delay time of a CR delay circuit, and wherein random variations of the resistance and the capacitor values of the CR delay circuit are used for generating the random signal. New Claim 19 is supported by the originally filed specification and does not add new matter.[2] Applicants respectfully submit that the '029 patent fails to disclose using random variations of resistance and capacitor values of the CR delay circuit for generating the random signal, as recited in new Claim 22. Accordingly, Applicants respectfully submit that new Claims 22-28 patentably define over the '029 patent.

Thus, it is respectfully submitted that independent Claims 1 and 22 (and all associated dependent claims) properly define over any proper combination of the '029 and '142 patents.

[2] See, e.g., original Figures 1 and 6 and the discussion related thereto in the specification, as well as original Claim 2. See also paragraph 34 in the published application.

Consequently, in view of the present amendment and in light of the above discussion, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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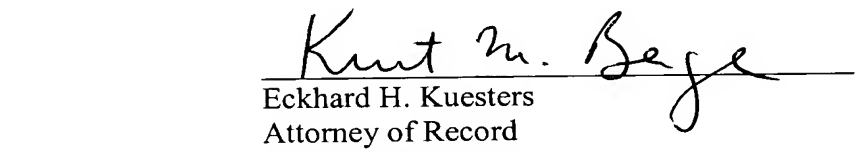

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